

What is claimed is:

1 1. A method of writing data to a row of single transistor memory cells wherein  
2 an applied gate voltage when writing a “0” is different than an applied gate voltage  
3 when writing a “1.”

1 2. The method of claim 1 wherein writing data comprises writing data to single  
2 transistor floating-body memory cells.

1 3. The method of claim 1 further comprising applying drain voltages to either  
2 charge or discharge bodies of the single transistor memory cells.

1 4. The method of claim 3 wherein applying a drain voltage to charge bodies  
2 comprises creating impact ionization currents.

1 5. The method of claim 3 wherein applying a drain voltage to discharge bodies  
2 comprises creating a voltage differential to turn on a diode.

1 6. The method of claim 1 wherein the applied gate voltage when writing a “0”  
2 is less than the applied gate voltage when writing a “1.”

1 7. A method comprising writing data to floating-body memory cells in two  
2 phases, wherein each of the two phases utilizes a different word line voltage on a  
3 word line.

1 8. The method of claim 7 wherein a first phase writes to a first subset of  
2 memory cells coupled to the word line.

1 9. The method of claim 8 wherein the first phase discharges floating bodies of  
2 the first subset of memory cells.

1 10. The method of claim 8 wherein the first phase comprises reducing a voltage  
2 on at least one bit line to turn on a diode formed at least partially by a floating body  
3 of a transistor.

1 11. The method of claim 8 wherein a second phase writes to a second subset of  
2 memory cells coupled to the word line.

1 12. The method of claim 11 wherein the second phase charges floating bodies of  
2 the second subset of memory cells.

1 13. The method of claim 11 wherein:  
2 the first phase includes providing a first drain voltage on the first subset of  
3 memory cells and a second drain voltage on cells other than the first subset; and  
4 the second phase includes providing a third drain voltage on the second  
5 subset of memory cells and a fourth drain voltage on cells other than the second  
6 subset.

1 14. A method comprising:  
2 providing a first voltage on a word line coupled to a plurality of memory  
3 cells;  
4 writing "0" to at least one of the plurality of memory cells;  
5 providing a second voltage on the word line; and  
6 writing "1" to at least one of the plurality of memory cells.

1 15. The method of claim 14 wherein each of the plurality of memory cells  
2 includes a single transistor.

1 16. The method of claim 15 wherein the word line is coupled to gates of the  
2 single transistors.

1 17. The method of claim 15 wherein the second voltage is higher than the first  
2 voltage.

1 18. The method of claim 14 wherein each of the plurality of memory cells  
2 comprises a floating-body transistor.

1 19. The method of claim 14 wherein writing a "0" comprises providing a voltage  
2 on a bit line to turn on a diode.

1 20. The method of claim 14 wherein writing a "1" comprises providing a voltage  
2 on a bit line to generate an impact ionization current.

1 21. An apparatus comprising:  
2 a row of memory cells; and  
3 a word line driver coupled to the row of memory cells, the word line driver  
4 to generate a first voltage when writing a "0" and a second voltage when writing a  
5 "1."

1 22. The apparatus of claim 21 wherein the word line driver is adapted to  
2 generate at least three different voltages.

1 23. The apparatus of claim 22 wherein the word line driver is adapted to  
2 generate at least four different voltages.

1 24. The apparatus of claim 21 wherein the row of memory cells comprise  
2 floating-body transistors.

1 25. A memory device comprising:  
2 floating-body single transistor memory cells;

3           a plurality of word line drivers coupled to the floating-body single transistor  
4 memory cells; and  
5           a plurality of bit line drivers coupled to the floating-body single transistor  
6 memory cells;  
7           wherein the memory device is adapted to perform two-phase writes in which  
8 the plurality of word line drivers drive a first voltage during a first phase to write  
9 one logical value, and the plurality of word line drivers drive a second voltage  
10 during a second phase to write a complementary logical value.

1   26.    The memory device of claim 25 wherein the word line drivers are adapted to  
2 drive the first voltage during the first phase when coupled to a selected row, and to  
3 drive a third voltage during the first phase when coupled to an unselected row.

1   27.    The memory device of claim 26 wherein the word line drivers are adapted to  
2 drive the second voltage during the second phase when coupled to a selected row,  
3 and to drive a fourth voltage during the second phase when coupled to an unselected  
4 row.

1   28.    An electronic system comprising:  
2           an antenna;  
3           a first integrated circuit coupled to the antenna; and  
4           a second integrated circuit including a memory device, the memory device  
5 comprising floating-body single transistor memory cells; a plurality of word line  
6 drivers coupled to the floating-body single transistor memory cells; and a plurality  
7 of bit line drivers coupled to the floating-body single transistor memory cells;  
8 wherein the memory device is adapted to perform two-phase writes in which the  
9 plurality of word line drivers drive a first voltage during a first phase to write one  
10 logical value, and the plurality of word line drivers drive a second voltage during a  
11 second phase to write a complementary logical value.

1 29. The electronic system of claim 28 wherein the word line drivers are adapted  
2 to drive the first voltage during the first phase when coupled to a selected row, and  
3 to drive a third voltage during the first phase when coupled to an unselected row.

1 30. The electronic system of claim 29 wherein the word line drivers are adapted  
2 to drive the second voltage during the second phase when coupled to a selected row,  
3 and to drive a fourth voltage during the second phase when coupled to an unselected  
4 row.